1. A single-pass packet processor for processing received packets comprising

a stateless segment comprising at least one pipelined plurality of stateless functional modules, each of said stateless functional modules performing stateless processing of received packets, and

a stateful segment comprising at least one pipelined plurality of stateful functional modules, each of said stateful functional modules performing stateful processing of packets that have been processed by at least one of said stateless functional units.

2. The single-pass packet processor of claim 1 further comprising a plurality of communications ports for sending and receiving packets.

3. The single-pass packet processor of claim 1 wherein said plurality of stateless functional modules comprises at least one stateless L2 ingress module for mapping an IP address of a received packet to at a corresponding L2 address.

4. The single-pass packet processor of claim 2 wherein said at least one stateless L2 ingress module performs L2 decapsulation of a received packet to derive an IP packet that is made available to at least one other of said stateless or stateful functional modules.

5. The single-pass packet processor of claim 4 wherein said plurality of stateless functional modules comprises at least one stateless L3 ingress module, said L3 ingress module comprising

means for checking the IP header of said IP packet for anomalies,

means for performing IP checksum verification on said IP packet,

means for storing a list of IP addresses associated with said single-pass packet processor, and

means for determining, based on said IP header and said list of IP addresses, whether the examined packet is to be retained at said packet processor or routed to another destination.

6. The single-pass packet processor of claim 5 further comprising